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100911.002700.1

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of U.S. Patent No. 6,526,469	) :)	Examiner: Not Yet Assigned
ROBERT ALLEN DREHMEL ET AL.	:)	Group Art Unit: 2181
Application No.: 10/747,820	:)	
Filed: December 30, 2003	:)	
For: BUS ARCHITECTURE EMPLOYING VARYING WIDTH UNI-DIRECTIONAL COMMAND BUS	:)	January 13, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION UNDER 37 C.F.R. § 1.173(c)

Sir:

Please find attached a table providing an explanation of the support in the disclosure of the original patent for the changes made to the claims.

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January 13, 2005
(Date of Deposit)

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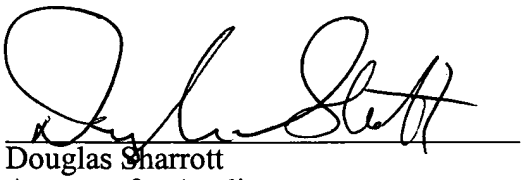
Signature

January 13, 2005
Date of Signature

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address given below.

Respectfully submitted,



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Claim	Support In Application No. 10/747,820
11. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a memory controller having an interface that includes a plurality of memory subsystem ports;	a memory controller includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101 and data switch (DSW) 211; the memory controller may also include address switch (ASW) 212 (Fig. 2A). ASW 212 or DSW 211 has at least two ports (Figs. 2A, 4 and 5) respectively interfacing with memory subsystems 203A and 203B (Fig. 2B). The memory controller initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines 16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;
a first memory subsystem including:	memory subsystem 203A or 203B:
a buffer device having a first port and a second port, and	a buffer device includes memory data interface (MDI) 221, with a first port (coupled to DSW 211) and a second port (coupled to a memory device), see Fig. 2B; the buffer device may also include memory address interface (MAI) 220, with a first port (coupled to ASW 212) and a second port (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a plurality of memory devices coupled to the buffer device via the second port, wherein data is transferred between at least one memory device of the plurality of memory devices and the memory controller via the buffer device; and	eight memory devices coupled to MDI 221 and MAI 220 via its second port (Fig. 2B); data is transferred between at least one memory device and the memory controller via MDI 221 and MAI 220 (Figs. 2A and 2B);

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a plurality of point-to-point links, each point-to-point link of the plurality of point-to-point links having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of point-to-point links including a first point-to-point link to connect the first port to a first memory subsystem port of the plurality of memory subsystem ports.	first and second point-to-point links (e.g., "bidirectional point-to-point remote data buses" 602 of Fig. 6, col. 10, lines 50-52, and "bus request/grant lines" 721/722 of Fig. 7, col. 12, lines 26-33), respectively connected to first and second memory subsystem ports of DSW 211, the first point-to-point link connecting the first port of MDI 221 to the first memory subsystem port of DSW 211; and first and second point-to-point links (e.g., "point-to-point send and receive status links" 403 and 404 of Fig. 4, col. 9, lines 1-7, and "point-to-point receive response links" 504 of Fig. 5, col. 9, lines 61-65), respectively connected to first and second memory subsystem ports of ASW 212, the first point-to-point link connecting the first port of MAI 220 to the first memory subsystem port of ASW 212.
12. The memory system of claim 11, further including: a plurality of connectors, wherein each connector of the plurality of connectors is connected to a respective point-to-point link of the plurality of point-to-point links; and a plurality of memory subsystems, and wherein each memory subsystem of the plurality of memory subsystems includes:	See col. 6, lines 49-53, and col. 21, lines 8-12, each memory subsystem card 203A or 203B has connectors at its boundary for respectively connecting to point-to-point links (403, 404, 504, 602, 721 and 722); and for memory subsystems 203A and 203B; see Fig. 2B; for additional memory subsystems, see also col. 20, lines 41-50, disclosing that a "larger number of devices" – such as memory subsystems – may be supported, e.g. by using additional switching chips, and col. 5, lines 61-67, disclosing that "the actual number and configuration of CPUs, buses and various other units may vary"; each memory subsystem includes:

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a buffer device having a first port and a second port, wherein the first port is coupled to a respective connector of the plurality of connectors; and a plurality of memory devices coupled to the buffer device via the second port.	a buffer device MDI 221 and MAI 220, having a first port and a second port, the first port being coupled to a respective connector at the memory card boundary; and eight memory devices coupled to MDI 221 and MAI 220 via the second port.
13. The memory system of claim 12, further including a plurality of substrates wherein each memory subsystem of the plurality of memory subsystems is disposed on a respective substrate of the plurality of substrates.	See col. 6, lines 49-55. Each memory subsystem card 203A and 203B may be separately packaged. See also col. 21, lines 1-7 (a "node," such as a memory subsystem, may be disposed on a card or chip).
14. The memory system of claim 11, wherein the first memory subsystem further includes a plurality of channels and a plurality of memory device select lines connected between the plurality of memory devices and the second port.	First memory subsystem 203A includes a plurality of channels and memory device select lines connected between the eight memory devices and the second port of MDI 221 and MAI 220 (see Fig. 2B, not all channels and select lines shown). See col. 6, line 57- col. 7, line 3, col. 8, lines 13-19.
15. The memory system of claim 14, wherein each channel of the plurality of channels includes a plurality of high speed terminated signal lines.	See col. 1, lines 19-22, disclosing "high-speed communication buses for linking processors, memory and other components;" col. 3, lines 21-22, disclosing "high-speed communication path architecture," and col. 21, lines 8-12, "communication access card boundary requires connectors, drivers, other hardware." Further, it was well known to those skilled in the computer arts at the time of the invention to always terminate high speed signal lines to reduce voltage reflections. See U.S. Patent 6,502,161, prior art Fig. 2A, showing terminated signal lines.
16. The memory system of claim 11, further including a second memory subsystem including:	Second memory subsystem 203B including:

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a buffer device having a first port and a second port, wherein the first port is connected to a second point-to-point link of the plurality of point-to-point links; and a plurality of memory devices coupled to the buffer device via the second port.	a buffer device comprising MDI 221 and MAI 220 (Fig. 2B), having a first port and a second port, wherein the first port is connected to a second point-to-point link (403, 404, 504, 602, 721 and 722); and eight memory devices coupled to second port of MDI 221 and MAI 220 (Fig. 2B).
17. The memory system of claim 11, further including a module substrate having a connector interface, wherein the first memory subsystem is disposed on the module substrate, and the buffer device is electrically connected to the connector interface, wherein the buffer device further comprises a memory address interface unit and transceives data, control and address signals between the plurality of memory devices and the connector interface.	Col. 6, lines 49-53; col. 21, lines 1-12, disclosing memory subsystem 203A or 203B disposed on a module substrate, for example, a card or chip, having a connector interface at the card or chip boundary, wherein the buffer device, comprising MDI 221 and memory address interface (MAI) unit 220, is electrically connected to the connector interface (see Fig. 2B), and the buffer device transceives data, control and address signals between memory devices and connector interface (see Figs. 2B and 3-7, wherein data, control and address signals to/from 305, 403, 404, 504, 602, 721 and 722 are transceived by the buffer device between the eight memory devices and the connector interface).
18. The memory system of claim 11, further including a first termination coupled to the first point-to-point link to terminate a first end of the first point-to-point link, wherein the first point-to-point link is a high speed link.	See claim 15 above.
19. The memory system of claim 18, further including a second termination coupled to the first point-to-point link to terminate a second end of the first point-to-point link.	See claim 15 above.

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20. The memory device of claim 11, wherein the buffer device comprises a write buffer, coupled to the first port, to hold data to be provided to at least one memory device of the plurality of memory devices.	The buffer device includes a write buffer MDI 221 coupled to the first port, to hold data to be provided to at least one of the eight memory devices; see col. 6, lines 63-65; see also col. 18, lines 9-10.
21. The system according to claim 11, wherein the buffer device comprises a memory data interface unit for transceiving data between at least one point-to-point link and at least one memory device.	The buffer device comprises a memory interface (MDI) unit 221 for transceiving data between at least one point-to-point link (602, 721 and 722); see Figs. 6, 7 and col. 6, lines 63-65.
22. The system according to claim 11, wherein the memory controller comprises a data switch for transceiving data to and from the first memory subsystem.	The memory controller includes a data switch (DSW) 211 for transceiving data to and from first memory subsystem 203A (see Figs. 2A, 2B, 6 and 7).
23. The system according to claim 13, wherein each substrate comprises a card or assembly of cards.	Col. 6, lines 49-54, which discloses that a substrate may comprise a card or an assembly of cards.
24. The system according to claim 11, wherein the first point-to-point link comprises a bidirectional point-to-point data bus.	Col. 10, lines 50-52: "Databus portion further contains a set of bidirectional point-to-point remote data buses 602A-602D running between DSW 211 and the memory subsystems 203;" see also Fig. 6.
25. A memory system comprising: a controller device;	See generally Figs. 1-7 and accompanying description: a controller device includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101 and data switch (DSW) 211; the memory controller may also include address switch (ASW) 212 (Fig. 2A). ASW 212 or DSW 211 interfaces with memory subsystems 203A and 203B (Fig. 2B). The controller device initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13,

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	lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines 16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;
a first buffer device having a first interface and a second interface;	in memory subsystem 203A, a first buffer device includes memory data interface (MDI) 221, with a first interface (coupled to DSW 211) and a second interface (coupled to a memory device), see Fig. 2B; the first buffer device may also include memory address interface (MAI) 220, with a first interface (coupled to ASW 212) and a second interface (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a second buffer device having a first interface and a second interface;	in memory subsystem 203B, a second buffer device includes MDI 221, with a first interface (coupled to DSW 211) and a second interface (coupled to a memory device), see Fig. 2B; the second buffer device may also include MAI 220, with a first interface (coupled to ASW 212) and a second interface (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a first point-to-point link having a first connection to the controller device and a second connection to the first interface of the first buffer device;	a first point-to-point link (e.g., "bidirectional point-to-point remote data buses" 602A/B of Fig. 6, col. 10, lines 50-52, and "bus request/grant lines" 721A/722A of Fig. 7, col. 12, lines 26-33), having a first connection to DSW 211 of the controller device, and a second connection to the first interface of the MDI 221 of the first buffer device of memory subsystem 203A; and a first point-to-point link (e.g., "point-to-point send and receive status links" 403A and 404A of Fig. 4, col. 9, lines 1-7, and "point-to-point receive response link" 504A of Fig.

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	5, col. 9, lines 61-65), having a first connection to ASW 212 of the controller device, and a second connection to the first interface of the MAI 220 of the first buffer device of memory subsystem 203A;
a first plurality of memory devices connected to the second interface of the first buffer device;	eight memory devices connected to the second interface of MDI 221 and MAI 220 of the first buffer device of memory subsystem 203A (Fig. 2B);
a second point-to-point link having a first connection to the controller device and a second connection to the first interface of the second buffer device; and	a second point-to-point link (e.g., "bidirectional point-to-point remote data buses" 602C/D of Fig. 6, col. 10, lines 50-52, and "bus request/grant lines" 721B/722B of Fig. 7, col. 12, lines 26-33), having a first connection to DSW 211 of the controller device and a second connection to the first interface of the second buffer device of memory subsystem 203B; and a second point-to-point link (e.g., "point-to-point send and receive status links" 403B and 404B of Fig. 4, col. 9, lines 1-7, and "point-to-point receive response links" 504B of Fig. 5, col. 9, lines 61-65), having a first connection to ASW 212 of the controller device and a second connection to the first interface of the second buffer device of memory subsystem 203B;
a second plurality of memory devices connected to the second interface of the second buffer device.	eight memory devices connected to the second interface of MDI 221 and MAI 220 of the second buffer device of memory subsystem 203B (Fig. 2B).
26. The memory system of claim 25, wherein the first buffer device and first plurality of memory devices are disposed on a first substrate, and the second buffer device and second plurality of memory devices are disposed on a second substrate.	Col. 6, lines 49-54 and col.21, lines 1-7, which disclose that each memory subsystem 203A and 203B may be disposed on a separate card or chip; the memory subsystem on each substrate includes a buffer device and eight memory devices (see claim 25).

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27. The memory system of claim 26, further including: a first plurality of high speed signal lines to connect the first plurality of memory devices to the second interface of the first buffer device; a second plurality of high speed signal lines to connect the second plurality of memory devices to the second interface of the second buffer device; a first plurality of termination elements connected to the first plurality of high speed signal lines; and a second plurality of termination elements connected to the second plurality of high speed signal lines.	See claims 14 and 15 above (disclosure concerning terminated high speed signal lines applies for both memory subsystems 203A and 203B of Fig. 2B)
28. The memory system of claim 25, further including a third point-to-point link having a connection to the controller and a fourth point-to-point link having a connection to the controller.	Third and fourth point-to-point links having a connection to the controller may include any one of links 403, 404, 504 (connected to ASW 212 of the controller) or links 602, 721 and 722 (connected to DSW 211 of the controller).
29. The memory system of claim 25, further including: a first channel to connect the first plurality of memory devices to the second interface of the first buffer device; a second channel to connect the second plurality of memory devices to the second interface of the second buffer device; a third channel connected to the second interface of the first buffer device; a third plurality of memory devices electrically coupled to the third channel; a fourth channel connected to the second interface of the second buffer device; and a fourth plurality of memory devices electrically coupled to the fourth channel.	See claim 14 above; see also Fig. 2B showing first and third channels respectively connecting "left" (first plurality) and "right" (third plurality) memory devices of memory subsystem 203A to second interface of first buffer device (MDI 221 and MAI 220), and second and fourth channels respectively connecting "left" (second plurality) and "right" (fourth plurality) memory devices of memory subsystem 203B to second interface of first buffer device (MDI 221 and MAI 220).

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30. The memory system of claim 25, further including at least one termination element electrically connected to the first point-to-point link, wherein the first point-to-point link is a high speed link.	See claim 15 above.
31. The memory system of claim 25, further including a module substrate having a connector interface, wherein the first buffer device is disposed on the module substrate, and the first buffer device is electrically connected to the connector interface, and wherein the first buffer device further comprises a memory address interface unit and transceives data, control and address information between the first plurality of memory devices and the connector interface.	See claim 17 above.
32. The memory device of claim 25, wherein the first buffer device further includes a write buffer, coupled to the first interface of the first buffer device, to hold data to be provided to at least one memory device of the first plurality of memory devices.	See claim 20 above.
33. A memory system comprising: a controller device;	See generally Figs. 1-7 and accompanying description: a controller device includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101. The controller device initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines 16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;

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a first and second plurality of buffer devices, each buffer device of the first and second plurality of buffer devices having an interface connected to a respective plurality of memory devices;	a first plurality of buffer devices includes the memory data interfaces (MDI) 221 of memory subsystems 203A and 203B, and the second plurality of buffer devices includes the memory address interfaces (MAI) 220 of memory subsystems 203A and 203B, each buffer device having an interface connected to a respective plurality of memory devices (see Fig. 2B); see also col. 6, lines 57-65;
a first and second repeater device;	a first repeater device comprising data switch (DSW) 211, and a second repeater device comprising address repeater (ARP) 210 and address switch (ASW) 212 (Fig. 2A). See also col 7, line 43, col. 10, lines 60-61;
a first point-to-point link having a first connection to the controller device and a second connection to the first repeater device;	see Fig. 2A (point-to-point link between CPU 101 and DSW 211); col. 6, lines 32-34;
a second point-to-point link having a first connection to the controller device and a second connection to the second repeater device;	see Fig. 2A (point-to-point link between CPU 101 and ARP 210/ASW 212); col. 6, lines 29-32;
a first plurality of repeater links, each repeater link having a first connection to a respective buffer device of the first plurality of buffer devices, and a second connection to the first repeater device; and	a first plurality of repeater links (602, 721 or 722) each repeater link having a first connection to MDI 221 (of memory subsystem 203A or 203B) and DSW 211;
a second plurality of repeater links, each repeater link having first connection to a respective buffer device of the second plurality of buffer devices and a second connection to the second repeater device.	a second plurality of repeater links (305, 403, 404 or 504), each repeater link having a first connection to MAI 220 (of memory subsystem 203A or 203B) and ARP 210/ ASW 212.
34. The memory system of claim 33, wherein a first buffer device of the first plurality of buffer devices and a first buffer device of the	MDI 221 (first buffer device of first plurality of buffer devices) and MAI 220 (first buffer device of second plurality of buffer

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second plurality of buffer devices, and corresponding pluralities of memory devices, are disposed on one of a plurality of respective module substrates.	devices), and memory devices of memory subsystem 203A are disposed on a substrate of a plurality of substrates; see Fig. 2B and col. 6, lines 49-54.
35. The memory system of claim 33, further including a third point-to-point link having an end connected to the controller device and a fourth point-to-point link having an end connected to the controller device.	See Fig. 2A (third and fourth point-to-point links with one end connected to CPU 101); col. 6, lines 29-34.
36. The memory device of claim 33, wherein each buffer device of the first plurality of buffer devices comprises a write buffer to hold data to be provided to at least one memory device of the respective plurality of memory devices.	See claim 20 above (first plurality of buffer devices comprise write buffers MDI 221).
37. The system according to claim 33, wherein each buffer device of the second plurality of buffer devices comprises a memory address interface unit for transceiving address information to and from at least one memory device.	See claim 33 above (second plurality of buffer devices comprise memory address interface (MAI) units 220, for transceiving address information to and from at least one memory device. Col. 6, lines 61-63.
38. The system according to claim 33, wherein the second repeater device comprises an address repeater unit for transceiving address information to and from the controller.	See claim 33 above (second repeater further includes address repeater (ARP) unit 210 for transceiving address information to and from the controller); col. 6, lines 29-32.
39. The system according to claim 38, wherein the second repeater device further comprises an address switch for transceiving the address information to and from the address repeater unit.	See claim 33 above (second repeater includes address switch (ASW) 212 for transceiving address information to and from ARP 210); col. 7, lines 4-7.
40. The system according to claim 33, wherein the second plurality of repeater links comprise an address bus for transmitting	See claim 33 above, and Fig. 3, address bus 305 for transmitting address information from the second repeater device ARP 210/

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address information from the second repeater unit to the second plurality of buffer devices, the address information being associated with data transceived between the first repeater device and the first plurality of buffer devices.	ASW 212 to the second plurality of buffer devices MAI 220, the address information being associated with data transceived between the first repeater device DSW 211 and the first plurality of buffer devices MDI 221; see also col. 6, line 61, to col. 7, line 3, and col. 8, lines 11-17.
41. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a controller device having an interface;	a controller device includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101 and data switch (DSW) 211; the memory controller may also include address switch (ASW) 212 (Fig. 2A). ASW 212 or DSW 211 interfaces with memory subsystems 203A and 203B (Fig. 2B). The controller device initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;
a first connector, second connector, and third connector;	see col. 6, lines 49-53, and col. 21, lines 8-12, three memory subsystems each have a connector at the card boundary for connecting to various point-to-point links (for example, links 403, 404, 504, 602, 721 and 722); two memory subsystems 203A and 203B (having first and second connectors) are shown in Fig. 2B; a third memory subsystem (not shown) is supported by col. 20, lines 41-50, disclosing that a "larger number of devices" – such as memory subsystems – may be supported, e.g. by using additional switching chips, and by col. 5, lines 61-67, disclosing that "the actual number and configuration of CPUs, buses and various other units may vary;" and

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	a memory subsystem card, such as memory subsystem 203A, has multiple (first, second and third) connectors at its boundary for connecting to various point-to-point links, such as links 403A, 404A, 504A, 602A, 602B, 721A and 722A;
a first point-to point link having a first connection to the interface and a second connection to the first connector;	a first point-to-point link (any one of links 403, 404, 504, 602, 721 and 722) connects DSW 211 or ASW 212, as the case may be, to the first connector of the first memory subsystem 203A; and a first point-to-point link (any one of links 403A, 404A, 504A, 602A, 602B, 721A and 722A) connects DSW 211 or ASW 212, as the case may be, to the first connector of memory subsystem 203A (Figs. 2A, 2B, 4, 5, 6 and 7);
a second point-to-point link having a first connection to the interface and a second connection to the second connector;	a second point-to-point link (any one of links 403, 404, 504, 602, 721 and 722) connects DSW 211 or ASW 212, as the case may be, to the second connector of the second memory subsystem 203B; and a second point-to-point link (any one of links 403A, 404A, 504A, 602A, 602B, 721A and 722A) connects DSW 211 or ASW 212, as the case may be, to the second connector of memory subsystem 203A (Figs. 2A, 2B, 4, 5, 6 and 7);
a third point-to-point link having a first connection to the interface and a second connection to the third connector; and	a third point-to-point link (any one of links 403, 404, 504, 602, 721 and 722) connects DSW 211 or ASW 212, as the case may be, to the third connector of the third memory subsystem (not shown, but disclosed as discussed above); and a third point-to-point link (any one of links 403A, 404A, 504A, 602A, 602B, 721A

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	and 722A) connects DSW 211 or ASW 212, as the case may be, to the third connector of memory subsystem 203A (Figs. 2A, 2B, 4, 5, 6 and 7);
a first memory subsystem including: a buffer device connected to the first connector; and a plurality of memory devices connected to the buffer device, wherein at least one memory device of the plurality of memory devices transfers data to the controller device via the buffer device.	a first memory subsystem 203A: a buffer device MDI 221 and MAI 220 connected to the first connector; eight memory devices connected to buffer device MDI 221 and MAI 220 of memory subsystem 203A (Fig. 2B), wherein at least one memory device transfers data to the controller device via the buffer device.
42. The memory system of claim 41, wherein the second and third connectors support coupling to a plurality of memory subsystems.	Second and third connectors respectively couple to a second memory subsystem 203B and a third memory subsystem (not shown but disclosed, as discussed in claim 41); and the first connector may be disposed on the first memory subsystem 203A, with the first point-to-point link connected thereto, and the second and third connectors may be disposed on the second memory subsystem 203B, with the second and third point-to-point links respectively connected thereto.
43. The memory system of claim 41, further including a module substrate having a connector interface, wherein the first memory subsystem is disposed on the module substrate, and the buffer device is electrically connected to the connector interface, and wherein the buffer device further comprises a memory address interface unit and transceives data, control and address signals between the plurality of memory devices and the connector interface.	See claim 17 above.

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44. The memory system of claim 41, further including a first termination to terminate the second connection of the first point-to-point link, wherein the first point-to-point link is a high speed link.	See claim 15 above.
45. The memory system of claim 44, further including a second termination to terminate the first connection of the first point-to-point link.	See claim 15 above.
46. The memory device of claim 41, wherein the buffer device comprises a write buffer to hold data to be provided to at least one memory device of the plurality of memory devices.	See claim 20 above.
47. A memory system comprising: a controller device; a plurality of buffer devices, each buffer device of the plurality of buffer devices having an interface connected to a respective plurality of memory devices; a repeater device;	See generally Figs. 1-7 and accompanying description: a controller device includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101. The controller device initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines 16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12; a plurality of buffer devices includes the memory data interfaces (MDI) 221 of memory subsystems 203A and 203B, each buffer device having an interface connected to a respective plurality of memory devices (see Fig. 2B); see also col. 6, lines 57-65; a first repeater device comprising data switch (DSW) 211. See also col. 10, lines 60-

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	61.
a point-to-point link having a first connection to the controller device and a second connection to the repeater device;	see Fig. 2A (point-to-point link between CPU 101 and DSW 211); col. 6, lines 32-34;
a plurality of repeater links, each repeater link having first connection to a respective buffer device of the plurality of buffer devices, and a second connection to the repeater device.	a plurality of repeater links (602, 721 or 722), each repeater link having a first connection to MDI 221 (of memory subsystem 203A or 203B) and DSW 211.
48. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a memory controller having an interface that includes a plurality of memory subsystem ports;	a memory controller includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101 and data switch (DSW) 211 (Fig. 2A). DSW 211 has at least two ports (Figs. 2A, 4 and 5) respectively interfacing with memory subsystems 203A and 203B (Fig. 2B). The memory controller initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines 16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;
a first memory subsystem including:	memory subsystem 203A or 203B:
a memory data interface unit having a first port and a second port, and	a memory data interface (MDI) 221, with a first port (coupled to DSW 211) and a second port (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a plurality of memory devices coupled to the memory data interface unit via the second port, wherein data is transferred between at	eight memory devices coupled to MDI unit 221 via its second port (Fig. 2B); data is transferred between at least one memory device and the memory controller via MDI

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least one memory device of the plurality of memory devices and the memory controller via the memory data interface unit; and	unit 221 (Figs. 2A and 2B);
a plurality of point-to-point links, each point-to-point link of the plurality of point-to-point links having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of point-to-point links including a first point-to-point link to connect the first port to a first memory subsystem port of the plurality of memory subsystem ports.	first and second point-to-point links (e.g., "bidirectional point-to-point remote data buses" 602 of Fig. 6, col. 10, lines 50-52, and "bus request/grant lines" 721/722 of Fig. 7, col. 12, lines 26-33), respectively connected to first and second memory subsystem ports of DSW 211, the first point-to-point link connecting the first port of MDI 221 to the first memory subsystem port of DSW 211.
49. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a controller device;	a controller device includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101 and data switch (DSW) 211. DSW 211 interfaces with memory subsystems 203A and 203B (Fig. 2B). The controller device initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines 16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;
a first memory data interface unit having a first interface and a second interface;	in memory subsystem 203A, a memory data interface (MDI) 221, with a first interface (coupled to DSW 211) and a second interface (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a second memory data interface unit having a first interface and a second interface;	in memory subsystem 203B, a second MDI 221, with a first interface (coupled to DSW 211) and a second interface (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;

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a first point-to-point link having a first connection to the controller device and a second connection to the first interface of the first memory data interface unit;	a first point-to-point link (e.g., "bidirectional point-to-point remote data buses" 602A/B of Fig. 6, col. 10, lines 50-52, and "bus request/grant lines" 721A/722A of Fig. 7, col. 12, lines 26-33), having a first connection to DSW 211 of the controller device, and a second connection to the first interface of the MDI 221 of the first buffer device of memory subsystem 203A;
a first plurality of memory devices connected to the second interface of the first memory data interface unit;	eight memory devices connected to the second interface of MDI 221 and MAI 220 of the first buffer device of memory subsystem 203A (Fig. 2B);
a second point-to-point link having a first connection to the controller device and a second connection to the first interface of the second memory data interface unit; and	a second point-to-point link (e.g., "bidirectional point-to-point remote data buses" 602C/D of Fig. 6, col. 10, lines 50-52, and "bus request/grant lines" 721B/722B of Fig. 7, col. 12, lines 26-33), having a first connection to DSW 211 of the controller device and a second connection to the first interface of the second buffer device of memory subsystem 203B;
a second plurality of memory devices connected to the second interface of the second memory data interface unit.	eight memory devices connected to the second interface of MDI 221 and MAI 220 of the second buffer device of memory subsystem 203B (Fig. 2B).
50. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a controller device;	a controller device includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101. The controller device initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines 16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus

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	master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;
a plurality of memory data interface units, each memory data interface unit of the plurality of memory data interface units having an interface connected to a respective plurality of memory devices;	a plurality of memory data interface (MDI) units 221 of memory subsystems 203A and 203B, each MDI unit having an interface connected to a respective plurality of memory devices (see Fig. 2B); see also col. 6, lines 57-65;
a repeater device;	a repeater device comprising data switch (DSW) 211. See also col. 10, lines 60-61.
a point-to-point link having a first connection to the controller device and a second connection to the repeater device;	see Fig. 2A (point-to-point link between CPU 101 and DSW 211); col. 6, lines 32-34.
a plurality of repeater links, each repeater link having first connection to a respective memory data interface unit of the plurality of memory data interface units, and a second connection to the repeater device.	a plurality of repeater links (602, 721 or 722) each repeater link having a first connection to MDI unit 221 (of memory subsystem 203A or 203B) and a second connection to DSW 211.
51. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a controller device having an interface;	a controller device includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101 and data switch (DSW) 211; the memory controller may also include address switch (ASW) 212 (Fig. 2A). ASW 212 or DSW 211 interfaces with memory subsystems 203A and 203B (Fig. 2B). The controller device initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;

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a first connector, second connector, and third connector;	see col. 6, lines 49-53, and col. 21, lines 8-12, three memory subsystems each have a connector at the card boundary for connecting to various point-to-point links (for example, links 403, 404, 504, 602, 721 and 722); two memory subsystems 203A and 203B (having first and second connectors) are shown in Fig. 2B; a third memory subsystem (not shown) is supported by col. 20, lines 41-50, disclosing that a "larger number of devices" – such as memory subsystems – may be supported, e.g. by using additional switching chips, and by col. 5, lines 61-67, disclosing that "the actual number and configuration of CPUs, buses and various other units may vary;" and a memory subsystem card, such as memory subsystem 203A, has multiple (first, second and third) connectors at its boundary for connecting to various point-to-point links, such as links 403A, 404A, 504A, 602A, 602B, 721A and 722A;
a first point-to point link having a first connection to the interface and a second connection to the first connector;	a first point-to-point link (any one of links 403, 404, 504, 602, 721 and 722) connects DSW 211 or ASW 212, as the case may be, to the first connector of the first memory subsystem 203A; and a first point-to-point link (any one of links 403A, 404A, 504A, 602A, 602B, 721A and 722A) connects DSW 211 or ASW 212, as the case may be, to the first connector of memory subsystem 203A (Figs. 2A, 2B, 4, 5, 6 and 7);
a second point-to-point link having a first connection to the interface and a second connection to the second connector;	a second point-to-point link (any one of links 403, 404, 504, 602, 721 and 722) connects DSW 211 or ASW 212, as the case may be, to the second connector of the second memory subsystem 203B; and

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	a second point-to-point link (any one of links 403A, 404A, 504A, 602A, 602B, 721A and 722A) connects DSW 211 or ASW 212, as the case may be, to the second connector of memory subsystem 203A (Figs. 2A, 2B, 4, 5, 6 and 7);
a third point-to-point link having a first connection to the interface and a second connection to the third connector; and	a third point-to-point link (any one of links 403, 404, 504, 602, 721 and 722) connects DSW 211 or ASW 212, as the case may be, to the third connector of the third memory subsystem (not shown, but disclosed as discussed above); and a third point-to-point link (any one of links 403A, 404A, 504A, 602A, 602B, 721A and 722A) connects DSW 211 or ASW 212, as the case may be, to the third connector of memory subsystem 203A (Figs. 2A, 2B, 4, 5, 6 and 7);
a first memory subsystem including: a memory data interface unit connected to the first connector; and a plurality of memory devices connected to the memory data interface unit, wherein at least one memory device of the plurality of memory devices transfers data to the controller device via the memory data interface unit.	a first memory subsystem 203A: a memory data interface (MDI) unit 221 connected to the first connector; eight memory devices connected to MDI 221 of memory subsystem 203A (Fig. 2B), wherein at least one memory device transfers data to the controller device via MDI 221.
52. A memory system comprising: a data switch having an interface that includes a plurality of memory subsystem ports; a first memory subsystem including:	See generally Figs. 1-7 and accompanying description: a data switch (DSW) 211 (Fig. 2A); see also col. 21, lines 1-12; memory subsystem 203A or 203B:

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a memory data interface unit having a first port and a second port, and	a memory data interface (MDI) unit 221, with a first port (coupled to DSW 211) and a second port (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a plurality of memory devices coupled to the memory data interface unit via the second port, wherein data is transferred between at least one memory device of the plurality of memory devices and the data switch via the memory data interface unit; and	eight memory devices coupled to MDI unit 221 via its second port (Fig. 2B); data is transferred between at least one memory device and the DSW 211 via MDI unit 221 (Figs. 2A and 2B);
a plurality of point-to-point links, each point-to-point link of the plurality of point-to-point links having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of point-to-point links including a first point-to-point link to connect the first port to a first memory subsystem port of the plurality of memory subsystem ports.	first and second point-to-point links (e.g., "bidirectional point-to-point remote data buses" 602 of Fig. 6, col. 10, lines 50-52, and "bus request/grant lines" 721/722 of Fig. 7, col. 12, lines 26-33), respectively connected to first and second memory subsystem ports of DSW 211, the first point-to-point link connecting the first port of MDI 221 to the first memory subsystem port of DSW 211.
53. A memory system comprising:	See generally Figs. 1-7 and accompanying description.
a data switch;	a data switch (DSW) 211 (Fig. 2A);
a first memory data interface unit having a first interface and a second interface;	in memory subsystem 203A, a first memory data interface (MDI) unit 221, with a first interface (coupled to DSW 211) and a second interface (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a second memory data interface unit having a first interface and a second interface;	in memory subsystem 203B, a second MDI unit 221, with a first interface (coupled to DSW 211) and a second interface (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a first point-to-point link having a first connection to the data switch and a second	a first point-to-point link (e.g., "bidirectional point-to-point remote data

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connection to the first interface of the first memory data interface unit;	buses" 602A/B of Fig. 6, col. 10, lines 50-52, and "bus request/grant lines" 721A/722A of Fig. 7, col. 12, lines 26-33), having a first connection to DSW 211 and a second connection to the first interface of the MDI unit 221 of memory subsystem 203A;
a first plurality of memory devices connected to the second interface of the first memory data interface unit;	eight memory devices connected to the second interface of the first MDI 221 of memory subsystem 203A (Fig. 2B);
a second point-to-point link having a first connection to the data switch and a second connection to the first interface of the second memory data interface unit; and	a second point-to-point link (e.g., "bidirectional point-to-point remote data buses" 602C/D of Fig. 6, col. 10, lines 50-52, and "bus request/grant lines" 721B/722B of Fig. 7, col. 12, lines 26-33), having a first connection to DSW 211 and a second connection to the first interface of the second MDI unit 221 of memory subsystem 203B;
a second plurality of memory devices connected to the second interface of the second memory data interface unit.	eight memory devices connected to the second interface of the second MDI unit 221 of memory subsystem 203B (Fig. 2B).
54. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a controller device;	a controller device includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for example, CPUs 101. The controller device initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines 16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;
a plurality of memory data interface units, each memory data interface unit of the plurality of memory data interface units	a first plurality of memory data interface (MDI) units 221 of memory subsystems 203A and 203B, each MDI unit 221 having an

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having an interface connected to a respective plurality of memory devices;	interface connected to a respective plurality of memory devices (see Fig. 2B); see also col. 6, lines 57-65;
a data switch;	a data switch (DSW) 211. See also col. 10, lines 60-61;
a point-to-point link having a first connection to the controller device and a second connection to the data switch;	see Fig. 2A (point-to-point link between CPU 101 and DSW 211); col. 6, lines 32-34;
a plurality of repeater links, each repeater link having first connection to a respective memory data interface unit of the plurality of memory data interface units, and a second connection to the data switch.	a plurality of repeater links (602, 721 or 722) each repeater link having a first connection to MDI unit 221 (of memory subsystem 203A or 203B), and a second connection to DSW 211.
55. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a data switch having an interface;	a data switch (DSW) 211 (Fig. 2A); see also col. 21, lines 1-12;
a first connector, second connector, and third connector;	see col. 6, lines 49-53, and col. 21, lines 8-12, three memory subsystems each have a connector at the card boundary for connecting to various point-to-point links (for example, links 602, 721 and 722); two memory subsystems 203A and 203B (having first and second connectors) are shown in Fig. 2B; a third memory subsystem (not shown) is supported by col. 20, lines 41-50, disclosing that a "larger number of devices" – such as memory subsystems – may be supported, e.g. by using additional switching chips, and by col. 5, lines 61-67, disclosing that "the actual number and configuration of CPUs, buses and various other units may vary;" and
	a memory subsystem card, such as memory subsystem 203A, has multiple (first,

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	second and third) connectors at its boundary for connecting to various point-to-point links, such as links 602A, 602B, 721A and 722A;
a first point-to point link having a first connection to the interface and a second connection to the first connector;	a first point-to-point link (any one of links 602, 721 and 722) connects DSW 211 to the first connector of the first memory subsystem 203A; and a first point-to-point link (any one of links 602A, 602B, 721A and 722A) connects DSW 211 to the first connector of memory subsystem 203A (Figs. 2A, 2B, 6 and 7);
a second point-to-point link having a first connection to the interface and a second connection to the second connector;	a second point-to-point link (any one of links 602, 721 and 722) connects DSW 211 to the second connector of the second memory subsystem 203B; and a second point-to-point link (any one of links 602A, 602B, 721A and 722A) connects DSW 211 to the second connector of memory subsystem 203A (Figs. 2A, 2B, 6 and 7); and
a third point-to-point link having a first connection to the interface and a second connection to the third connector; and	a third point-to-point link (any one of links 602, 721 and 722) connects DSW 211 to the third connector of the third memory subsystem (not shown, but disclosed as discussed above); and a third point-to-point link (any one of links 602A, 602B, 721A and 722A) connects DSW 211 to the third connector of memory subsystem 203A (Figs. 2A, 2B, 6 and 7);
a first memory subsystem including:	a first memory subsystem 203A:
a memory data interface unit connected to the first connector; and	a memory data interface (MDI) unit 221 connected to the first connector;
a plurality of memory devices connected to the memory data interface unit, wherein at	eight memory devices connected to MDI unit 221 of memory subsystem 203A (Fig.

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least one memory device of the plurality of memory devices transfers data to the data switch via the memory data interface unit.	2B), wherein at least one memory device transfers data to DSW 211 via MDI unit 221.
56. A memory system comprising: a data switch having an interface that includes a plurality of memory subsystem ports; a first memory subsystem including: a memory data interface unit having a first port and a second port, and a plurality of memory devices coupled to the memory data interface unit via the second port, wherein data is transferred between at least one memory device of the plurality of memory devices and the data switch via the memory data interface unit; and a plurality of bidirectional point-to-point data buses, each bidirectional point-to-point data bus of the plurality of bidirectional point-to-point data buses having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of bidirectional point-to-point data buses including a first bidirectional point-to-point data bus to connect the first port to a first memory subsystem port of the plurality of memory subsystem ports.	See generally Figs. 1-7 and accompanying description: a data switch (DSW) 211 (Fig. 2A); see also col. 21, lines 1-12; memory subsystem 203A or 203B: a memory data interface (MDI) unit 221, with a first port (coupled to DSW 211) and a second port (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65; eight memory devices coupled to MDI unit 221 via its second port (Fig. 2B); data is transferred between at least one memory device and DSW 211 via MDI unit 221 (Figs. 2A and 2B); first and second bidirectional point-to-point data buses (e.g., "bidirectional point-to-point remote data buses" 602 of Fig. 6, col. 10, lines 50-52), respectively connected to first and second memory subsystem ports of DSW 211, the first bidirectional point-to-point data bus connecting the first port of MDI 221 to the first memory subsystem port of DSW 211.
57. A memory system comprising: a data switch;	See generally Figs. 1-7 and accompanying description: a data switch (DSW) 211 (Fig. 2A);

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a first memory data interface unit having a first interface and a second interface;	in memory subsystem 203A, a first memory data interface (MDI) unit 221, with a first interface (coupled to DSW 211) and a second interface (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a second memory data interface unit having a first interface and a second interface;	in memory subsystem 203B, a second MDI unit 221, with a first interface (coupled to DSW 211) and a second interface (coupled to a memory device), see Fig. 2B; see also col. 6, lines 57-65;
a first bidirectional point-to-point data bus having a first connection to the data switch and a second connection to the first interface of the first memory data interface unit;	a first bidirectional point-to-point data bus (e.g., "bidirectional point-to-point remote data buses" 602A/B of Fig. 6, col. 10, lines 50-52), having a first connection to DSW 211 and a second connection to the first interface of the MDI unit 221 of memory subsystem 203A;
a first plurality of memory devices connected to the second interface of the first memory data interface unit;	eight memory devices connected to the second interface of the first MDI 221 of memory subsystem 203A (Fig. 2B);
a second bidirectional point-to-point data bus having a first connection to the data switch and a second connection to the first interface of the second memory data interface unit; and	a second bidirectional point-to-point data bus (e.g., "bidirectional point-to-point remote data buses" 602C/D of Fig. 6, col. 10, lines 50-52), having a first connection to DSW 211 and a second connection to the first interface of the second MDI unit 221 of memory subsystem 203B;
a second plurality of memory devices connected to the second interface of the second memory data interface unit.	eight memory devices connected to the second interface of the second MDI unit 221 of memory subsystem 203B (Fig. 2B).
58. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a controller device;	a controller device includes processor 201 (Fig. 2A, col. 6, lines 19-35), comprising, for

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	example, CPUs 101. The controller device initiates transfers to memory subsystems 203 (col. 11, lines 60-61, col. 13, lines 8-9), and otherwise controls memory (see, for example, col. 4, lines 26-27, col. 7, lines 16-32, col. 8, lines 11-15, col. 12, lines 10-33 and 62-65, and description of the processor as a "bus master" at col. 13, lines 10 *et seq.*); see also col. 21, lines 1-12;
a plurality of memory data interface units, each memory data interface unit of the plurality of memory data interface units having an interface connected to a respective plurality of memory devices;	a first plurality of memory data interface (MDI) units 221 of memory subsystems 203A and 203B, each MDI unit 221 having an interface connected to a respective plurality of memory devices (see Fig. 2B); see also col. 6, lines 57-65;
a data switch;	a data switch (DSW) 211; see also col. 10, lines 60-61;
a point-to-point link having a first connection to the controller device and a second connection to the data switch;	see Fig. 2A (point-to-point link between CPU 101 and DSW 211); col. 6, lines 32-34.
a plurality of bidirectional point-to-point data buses, each bidirectional point-to-point data bus having first connection to a respective memory data interface unit of the plurality of memory data interface units, and a second connection to the data switch.	a plurality of bidirectional point-to-point data buses (602), each bidirectional point-to-point data bus having a first connection to MDI unit 221 (of memory subsystem 203A or 203B), and a second connection to DSW 211.
59. A memory system comprising:	See generally Figs. 1-7 and accompanying description:
a data switch having an interface;	a data switch (DSW) 211 (Fig. 2A); see also col. 21, lines 1-12;
a first connector, second connector, and third connector;	see col. 6, lines 49-53, and col. 21, lines 8-12, three memory subsystems each have a connector at the card boundary; two memory subsystems 203A and 203B (having first and second connectors) are shown in Fig. 2B; a

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	third memory subsystem (not shown) is supported by col. 20, lines 41-50, disclosing that a "larger number of devices" – such as memory subsystems – may be supported, e.g. by using additional switching chips, and by col. 5, lines 61-67, disclosing that "the actual number and configuration of CPUs, buses and various other units may vary;" and a memory subsystem card, such as memory subsystem 203A, has multiple (first, second and third) connectors at its boundary;
a first bidirectional point-to point data bus having a first connection to the interface and a second connection to the first connector;	a first bidirectional point-to-point data bus (602) connects DSW 211 to the first connector of the first memory subsystem 203A; and a first bidirectional point-to-point data bus (602A) connects DSW 211 to the first connector of memory subsystem 203A (Figs. 2A, 2B and 6);
a second bidirectional point-to-point data bus having a first connection to the interface and a second connection to the second connector;	a second bidirectional point-to-point data bus (602) connects DSW 211 to the second connector of the second memory subsystem 203B; and a second bidirectional point-to-point data bus (602B) connects DSW 211 to the second connector of memory subsystem 203A (Figs. 2A, 2B and 6);
a unidirectional memory data bus line having a first connection to the interface and a second connection to the third connector; and	a unidirectional memory data bus line (721 or 722; see col. 12, lines 26-33) connects DSW 211 to the third connector of the third memory subsystem (not shown, but disclosed as discussed above); and a unidirectional memory data bus line (721A or 722A; see col. 12, lines 26-33) connects DSW 211 to the third connector of

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	memory subsystem 203A (Figs. 2A, 2B and 7);
a first memory subsystem including:	a first memory subsystem 203A:
a memory data interface unit connected to the first connector; and	a memory data interface (MDI) unit 221 connected to the first connector;
a plurality of memory devices connected to the memory data interface unit, wherein at least one memory device of the plurality of memory devices transfers data to the data switch via the memory data interface unit.	eight memory devices connected to MDI unit 221 of memory subsystem 203A (Fig. 2B), wherein at least one memory device transfers data to DSW 211 via MDI unit 221.